CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a die including

a plurality of bond pads configured in an array,

a first plurality of driver cells located between a nearest die edge and the plurality of bond pads, and

a second plurality of driver cells located to the inside of the plurality of bond pads; and

a lead frame including a plurality of lead fingers, the plurality of lead fingers coupled the plurality of bond pads by a plurality of bond wires.

2. The semiconductor device of claim 1, wherein the plurality of bond pads are configured in a staggered array.

3. The semiconductor device of claim 2, further comprising a plurality of pre-drive cells located farther from the nearest die edge than the second plurality of driver cells.

4. The semiconductor device of claim 3, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.

5. The semiconductor device of claim 4, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

6. The semiconductor device of claim 5, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

7. The semiconductor device of claim 6, wherein each of the plurality of conductive interconnects is substantially more narrow in width than each of the plurality of metal connections.

8. The semiconductor device of claim 7, wherein the first and second pluralities of driver cells each have a width of approximately 80 microns.

9. A semiconductor device, comprising:

a die including

a plurality of bond pads configured in an array,

a first plurality of driver cells located between a nearest die edge and the plurality of bond pads, and

a second plurality of driver cells located to the inside of the plurality of bond pads; and

a lead frame including a plurality of solder balls, the plurality of solder balls coupled the plurality of bond pads by a plurality of bond wires.

10. The semiconductor device of claim 9, wherein the plurality of bond pads are configured in a staggered array.

11. The semiconductor device of claim 10, further comprising a plurality of pre-drive cells located farther from the nearest die edge than the second plurality of driver cells.

12. The semiconductor device of claim 11, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.

13. The semiconductor device of claim 12, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

14. The semiconductor device of claim 13, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

15. The semiconductor device of claim 14, wherein each of the plurality of conductive interconnects is substantially more narrow in width than each of the plurality of metal connections.

16. The semiconductor device of claim 15, wherein the first and second pluralities of driver cells each have a width of approximately 80 microns.